harmonic modulator for use in this phased array. An advantage of using even-harmonic mixers in the direct I&Q modulator is the achievement of excellent carrier suppression by virtue of the cancellation of the even-harmonic currents in the anti-parallel diode pairs [3]. Also, lower cost and more readily available oscillators can be used since the LO frequency is half that of a conventional modulator. This system will require small, low-cost RF components capable of being manufactured in large quantities if cost of the phased array is to be kept reasonable. MMICs offer a potential solution to such large volume requirements. The MMIC modulator circuit was designed with the OMMIC's ED02AH foundry process and uses two pairs of 0.18 μm PHEMT based diodes, each having two 15 μm cathode fingers. The chip measures 2.9×1.7 mm^2 and is shown in Fig. 1.

II. Circuit Design

Development of the quadrature modulator, depicted in the block diagram in Fig. 2, requires the integration of two identical even-harmonic upconverters, a 90°-hybrid coupler, and a Wilkinson power divider. Details of each of these circuits are presented in the following section.

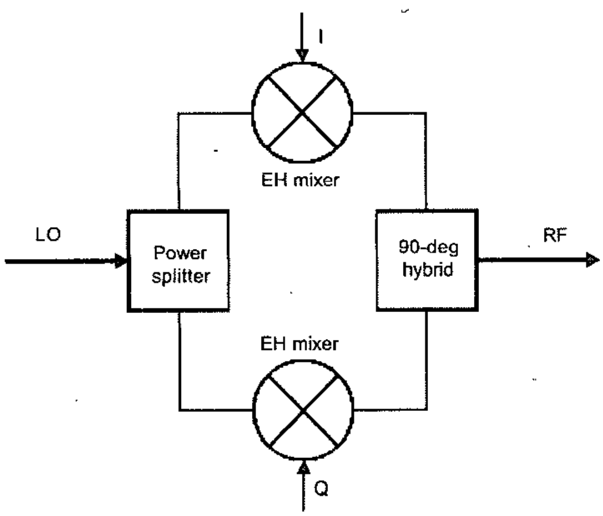

Fig. 2. Block diagram of the I&Q modulator.

III. Subharmonic Mixer

One of the critical components in a communications system is the mixer. In the transmit channel, it is important for the upconverter to have excellent carrier suppression properties. An advantage of the subharmonically pumped (SHP) mixer (also called the even-harmonic mixer) is a high 2·LO-RF suppression by virtue of the cancellation of the even-harmonic currents in the anti-parallel diode pair [4]. The LO-to-RF suppression is also high due to the large frequency separation between the LO and RF signals. Furthermore, with a SHP mixer, lower cost and better phase noise oscillators can be used since the LO frequency is half that of a conventional mixer.

Each even-harmonic (EH) upconverter is optimized to mix the I&Q baseband signals (DC to 200 MHz) with the second harmonic of the 21.75-to-22.75 GHz LO to provide a 43.5-to-45.5 GHz double sideband suppressed carrier (DSBSC) output signal at the RF port ($2f_{LO}\ \ f_{IF}$). An anti-parallel Schottky diode pair is used to provide cancellation of the even-harmonic LO currents, which minimizes $2f_{LO}$ leakage and suppresses the fundamental mixing products ($mf_{LO}\ \ nf_{IF}$) where m+n is even [5].

A layout of the modulator is shown in Fig. 1 with the upconverter subcircuit represented inside the dashed outline. The LO signal is applied at point "Y". The short-circuit stub "SCS" has a length of $\lambda_{LO}/4$, which acts as an open-circuit to the LO frequency but shorts out $2f_{LO}$ and f_{RF} (since $2f_{LO} \cong f_{RF}$ for this circuit). This is used to suppress the RF signal at the LO port and also provides a DC and IF return path. The $\lambda_{LO}/4$ open-circuit stub "OCS", connected at point "X", provides a virtual ground (and return path) at the LO frequency and also prevents LO leakage into the IF and RF ports. At $2f_{LO}$ and f_{RF}, the stub appears as an open-circuit and does not affect the RF signal. The RF parallel coupled-line bandpass filter (BPF) is used to extract the RF signal. Its passband was designed to cover the RF band of 43.5 to 45.5 GHz. This filter appears as a high impedance to the IF signal in order to provide good IF-RF isolation. Due to the large frequency separation between the LO and RF, the BPF also assists in attenuating the LO signal. The IF signal is injected at the IF port via the RF bandstop and lowpass filter (LPF). It consists of a shunt capacitance, followed by a CPW line, which is $\lambda_{RF}/4$ in length. This combination provides a high impedance at point "X" at the RF frequency, thus preventing the RF signal from appearing at the IF port. Distributed matching circuits (M1 and BPF) were designed to match the diode impedance at the LO and RF frequency to 50 Ω.

IV. Branch-Line 90° Hybrid

The DSBSC signal from each EH upconverter is applied to each input port of the quadrature (90°) hybrid and the combined RF output results in a single sideband RF signal. The amount of suppression of the unwanted sideband is strongly dependent on the amount of amplitude and phase imbalance of the 90° hybrid, as well as the symmetry between the two mixers. The quadrature hybrid was designed using Momentum [6], an electromagnetic (EM) field simulator. The topology is that of a standard branch-line hybrid comprised of quarter-wave long (at 44.5 GHz) 50-Ω and 35-Ω CPW line sections, shown in Fig. 1. The 50-Ω MMIC resistor at the isolated port is terminated to ground. The hybrid layout was optimized to ensure minimum amplitude and quadrature phase error between the two output ports. The simulation revealed less than 1.4 dB of amplitude and 2° of phase error over the 43.5 to 45.5 GHz RF band. Simulation of the port return loss and isolation were both better then 23 dB over the RF range.

V. WILKINSON POWER DIVIDER

The LO signal (f_{LO}) is split in-phase via the Wilkinson power divider and applied with equal amplitude to the LO port of each mixer, as shown in Fig. 1. Design of the two-way, equal split, power divider was simulated. This circuit consists of two equal lengths, 70-Ω assymmetric coplanar strip (ACPS) lines, each a quarter-wave long at the fundamental LO center frequency (22.25 GHz). The 100-Ω monolithic balancing resistor between the two output ports affects the port-to-port isolation and return loss of the output ports. The isolation between the two output ports and return loss of this circuit was predicted to be better than 28 dB and 22 dB respectively, over the 21.75-to-22.75 GHz LO range.

VI. MODULATOR LAYOUT

The layout of the two mixers, power divider and quadrature hybrid required careful planning to ensure optimum symmetry between the two mixers, minimum parasitic coupling between components and minimum GaAs substrate area. Several iterations of the circuit layout were required to arrive at the best layout in terms of minimum area and best performance. The local oscillator pump (or sub-harmonic of the RF carrier) is split in-phase and is applied to each mixer LO port. I&Q baseband signals (in-phase and quadrature) are applied to each mixer IF port. The RF output (DSBSC) from each upconverter is combined in the 90° hybrid where one of the sidebands is cancelled. The carrier ($2f_{LO}$) suppression is achieved within each anti-parallel diode pair.

VII. MODULATOR PERFORMANCE

The modulator was measured on a semi-automatic wafer prober with coplanar (ground-signal-ground) probes and was found to provide optimum performance at an LO power of 11 dBm. The conversion loss was measured to be 9 ± 0.6 dB across the RF bandwidth of 43.5 – 45.5 GHz. Since the desired output was a single sideband, suppressed carrier signal, the suppression of both the lower sideband (LSB) and the second harmonic of the LO was important. Fig. 3 shows that, in comparison to the desired upper sideband signal, the LSB was suppressed by at least 25 dB over the RF band of interest, $2\times f_{LO}$ was suppressed by about 15 dB and the 3rd order intermodulation (IM3) ($2f_{LO}-3f_{IF}$) suppression is better than 38 dB. The results shown were obtained with an IF frequency of 50 MHz but the chip operates with similar performance for I&Q frequencies up to 200 MHz as shown in Fig. 4.

VIII. CONCLUSION

The design and performance of a 44.5 GHz direct modulator MMIC with DC-to-200 MHz I&Q frequencies, developed in CPW has been described. The modulator converts baseband I & Q signals directly to 44.5 GHz, using the second harmonic of a 22.25 GHz local oscillator signal. The circuit incorporates two pairs of anti-parallel diodes to reduce the $2\times f_{LO}$ feedthrough. This 2.9 × 1.7 mm^2 chip was developed for use in a transmit phased array for an EHF satcom terminal. Measured results show good performance over the frequency band.

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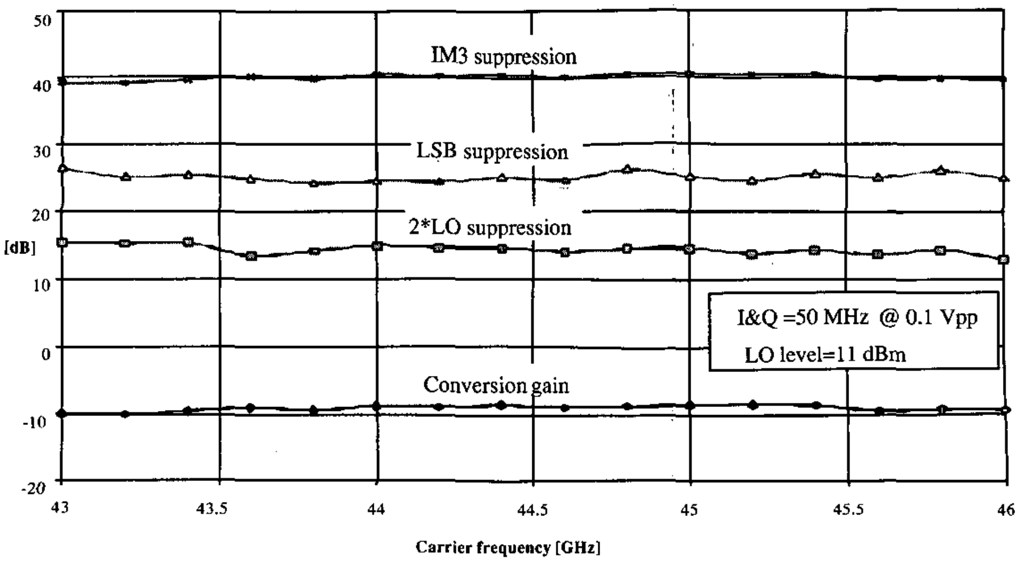

Fig. 3. Modulator Measured Performance versus RF Frequency

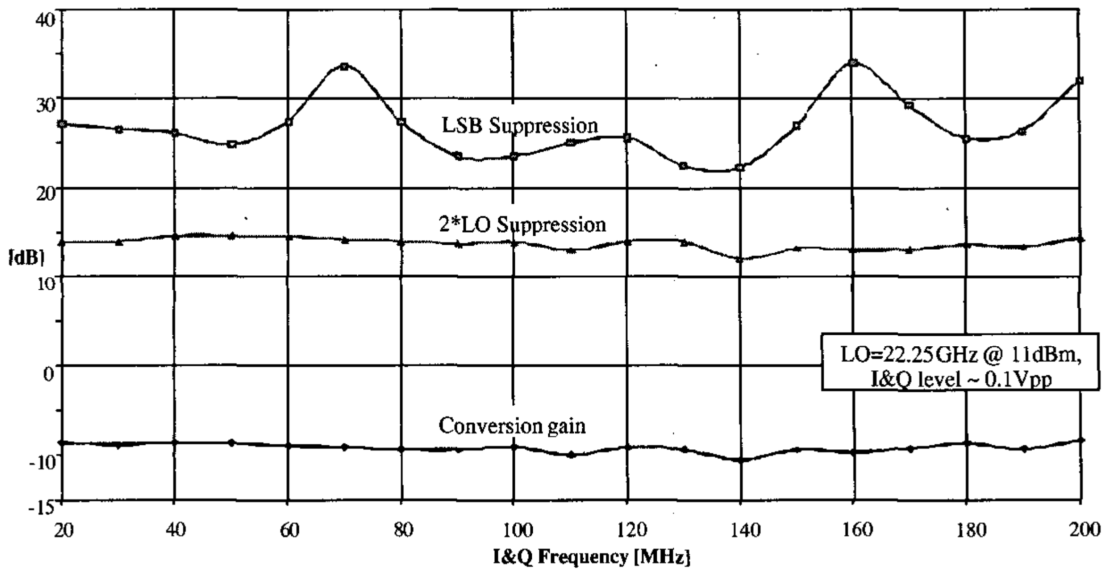

Fig. 4. Modulator Measured Performance versus I&Q Frequency